Introduction to Digital Logic

EECS/CSE 31L

**Assignment 1: 1-Bit Comparator**

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**1 Block Description**

This block is designed to take in 2 inputs in order to select between another 4 inputs

**2 Input/Output Port Description**

|  |  |  |  |
| --- | --- | --- | --- |
| Port name | Port size | Port Type | Description |
| Input0 | 1 | IN | Value of first input |
| Input1 | 1 | IN | Value of second input |
| Greater | 1 | OUT | First operation result |
| Equal | 1 | OUT | Second operation result |
| Less | 1 | OUT | Third operation result |

**3 Design Schematics**

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| In\_0 | In\_1 | Greater | Equal | Less |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |

**Boolean Expressions:**

Greater = (In\_0)(In\_1’)

Equal = (In\_0’)(In\_1’) + (In\_0)(In\_1) = In\_0 ⊙ In\_1

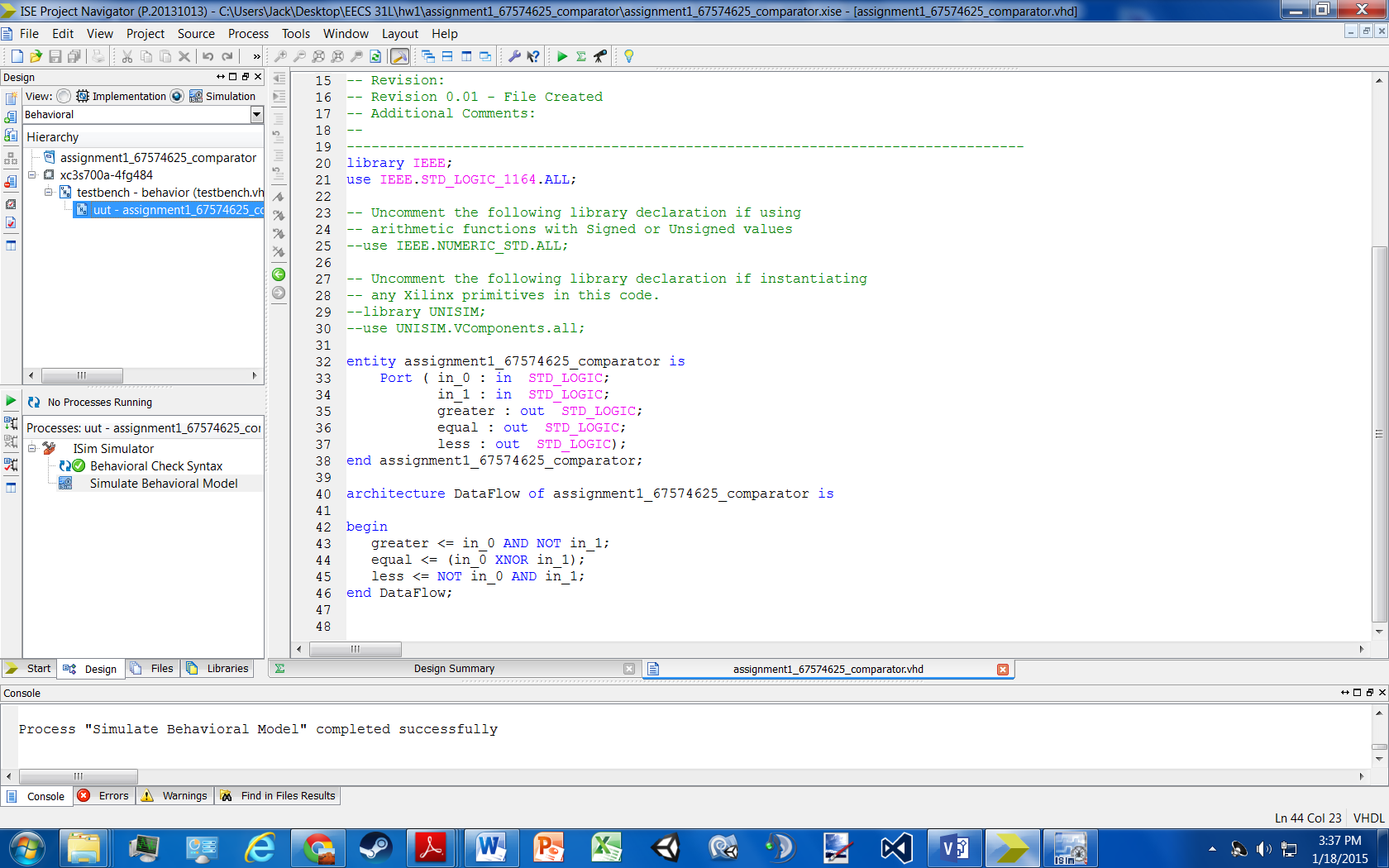
Less = (In\_0’)(In\_1)

**Gate Representation:**

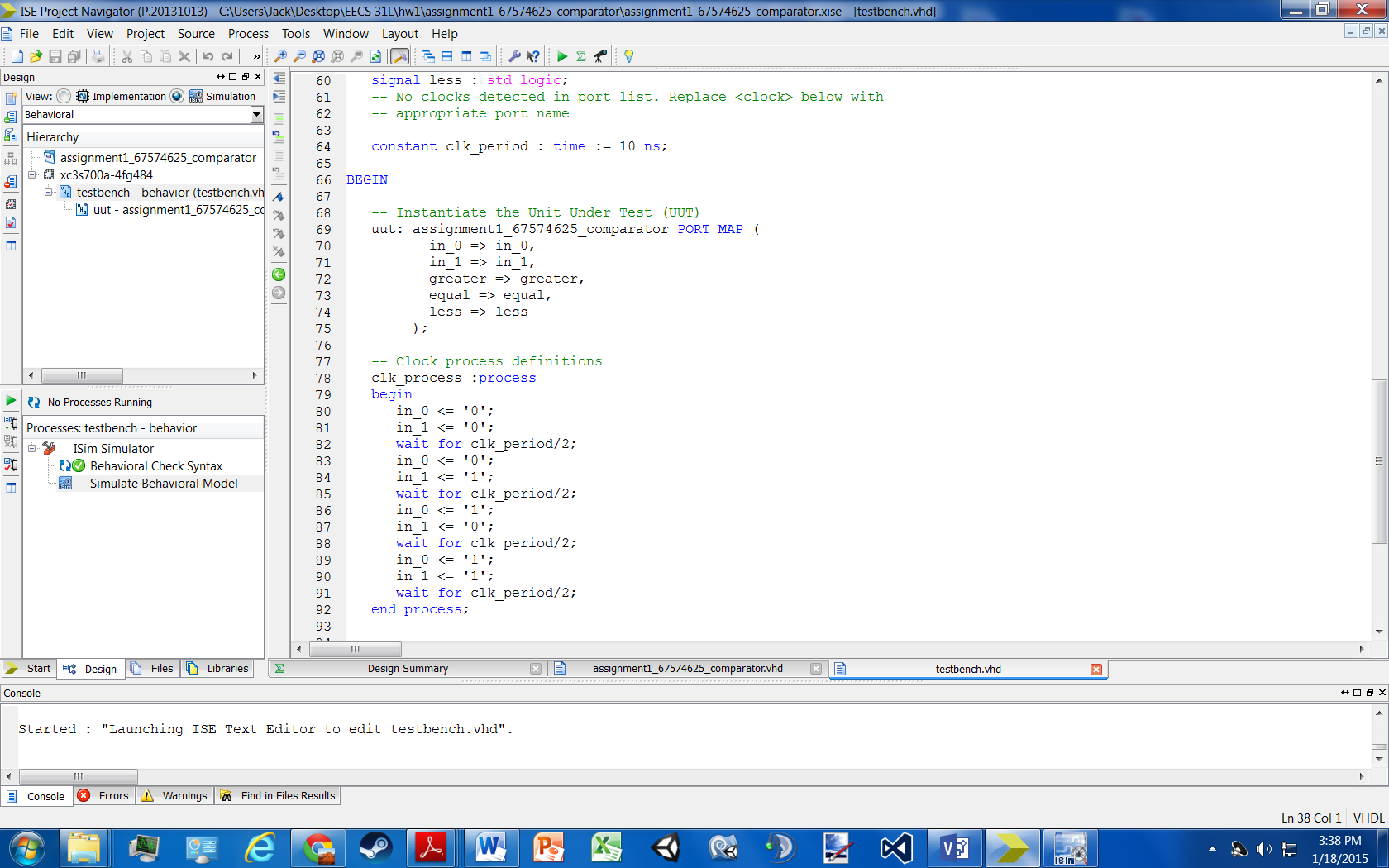


**4 Compilation**

Comparator compiled



Testbench compiled



**5 Elaboration**

**Assumptions:**

* All inputs and outputs are 1-Bit
* Less = 1 when in\_0 < in\_1 (‘0’ < ‘1’)
* Greater = 1 when in\_0 > in\_1 (‘1’ > ‘0’)
* Equal = 1 when in\_0 = in\_1 (‘0’ = ‘0’ or ‘1’ = ‘1’)

**Errors:**

* No errors occurred while coding

**Simulation Log:**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_beh.prj work.testbench

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/assignment1\_67574625\_comparator.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling architecture dataflow of entity assignment1\_67574625\_comparator [assignment1\_67574625\_comparator\_...]

Compiling architecture behavior of entity testbench

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 5 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_isim\_beh.exe

Fuse Memory Usage: 29860 KB

Fuse CPU Usage: 389 ms

Launching ISim simulation engine GUI...

"C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_comparator/testbench\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

**6 Waveform**

